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On-Chip Spiral Inductors and On-Chip Spiral Transistors for Accurate Numerical Modeling

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This paper presents a new model for designing on-chip spiral inductor and on-chip spiral transistors. For this, the coupling between on-chip inductors and transistors has been implemented. The electromagnetic coupling between the inductors and the transistors and the mutual inductance are modeled by presenting the magnetic vector potential to study the coupling effect. It changes the surface integral of the magnetic field into the loop integral of the magnetic vector potential to calculate the coupling. In this method, the partial mutual inductance idea to compute the mutual inductance between two conductor sections instead of conductor loops can be developed. The inductance classification is applied to an on-chip environment to characterize interconnects and integrated inductors. The investigative model is reconsidered to incorporate the semiconductor substrate losses and the skin effect. The numerical solutions of the investigative model are also presented. To simulate the proposed model ADS Momentum software is used.

Keywords : mutual inductance, magnetic field, magnetic flux, numerical solution

1. Introduction

Advanced semiconductor technologies have brought faster operating speed and a higher level of system integration in integrated circuits. In contrast, electromagnetic effects are associated with on-chip evolutions. In an on-chip environment, all circuit components share a common substrate, which are a semiconductor and not a perfect dielectric. This semiconductor substrate is associated with significant parasitic resistance, capacitance, and inductance. Thus, it establishes a complicated connection between circuit components, although they are not connected directly. Once the operating frequency of the circuit devices becomes higher, the substrate parasitic becomes more significant and the coupling between devices through substrate becomes stronger [1-4].

VLSI designers are focusing on achieving higher chip density; thus, with advanced technology, the spacing between the integrated circuit components decreases considerably. Devices operating at high frequencies and carrying high power signals leak large amounts of electric and magnetic energy into the surroundings. The electric and magnetic fields can directly couple to nearby devices and induce noise voltage and current [5-8]. In this study, the on-chip electromagnetic coupling is investigated for spiral inductor and transistor, and its performance is analyzed. The design tool presented in this work is a useful tool that provides independence from full-wave solvers. The ADS Momentum simulator that computes the S-parameters for general planar circuits.

2. The Scatter Parameters

The benefit of using Scattering parameters (*S* parameters) is that they can be straightforwardly measured by instruments. In any case, voltage and current cannot be measured directly at microwave frequencies. Rather, field and power can be measured specifically. Consequently, *S* parameters are clearer than impedance (*Z* Parameters) and admittance parameters (*Y* Parameters) and can be used to analyze high-frequency electric networks. *Z* and *Y* Parameters can be derived from *S* Parameters, as shown below:

$$\bar{Z} = (\bar{I} + \bar{S})(\bar{I} - \bar{S})^{-1} \quad (1)$$

where *Z* is impedance parameter and *Y* is admittance

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parameter

$$\overline{Y} = \overline{Z}^{-1} \tag{2}$$

In a two-port network, the S matrix is given by

$$\overline{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{3}$$

where the four S parameters are characterized as

$$V_1^{-1} = S_{11}V_1^+ + S_{12}V_2^+$$
$$V_2^{-1} = S_{21}V_1^+ + S_{22}V_2^+ \tag{4}$$

S_{11} is the insertion loss of Port 1 when Port 2 is matched while S_{21} is the forward gain from Port 1 to Port 2 when Port 2 is matched. S_{22} is the insertion loss of Port 2 when Port 1 is matched while S_{12} is the forward gain from Port 2 to Port 1 when Port 1 is matched.

For a symmetric network,

$$S_{11} = S_{22}$$
$$S_{12} = S_{21} \tag{5}$$

S parameters are frequently used for networks operating at radio frequency and microwave frequencies where signal power and energy concerns are simply quantified and compared to currents and voltages. S parameters change with the measurement frequency, so frequency must be specified for any S parameter measurements stated [9, 10].

This work uses simulation model based on dividing the geometry of the inductors and transistors into the segmented elements of an interface network that includes line spacing, line width, and number of turns. The usage of ADS Momentum software is calculation of various parameters like S_{11} Parameter, return losses, directivity, efficiency and gain of the proposed system.

3. Coupling between On-Chip Spiral Inductors

On-chip inductors have huge physical dimensions associated with important magnetic energy leakage. Since they are commonly utilized in analog radio-frequency circuits and work in the gigahertz range, the electromagnetic coupling between two spiral inductors needs to be investigated.

Planar coupling between two side-by-side spiral inductors on the same metal layer has been experimentally studied in [11] and a maximum $|S_{21}|$ of –25 dB has been observed at 1.5 GHz. The physical dimensions of the spiral inductors are shown in 1. The total number of turns is six,

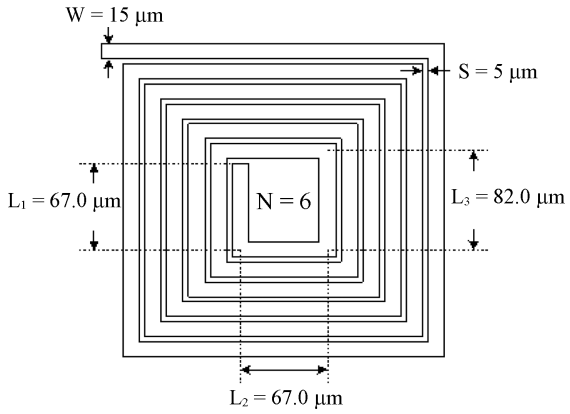

Fig. 1. Physical Dimensions of the Coupled Spirals in the Transformer.

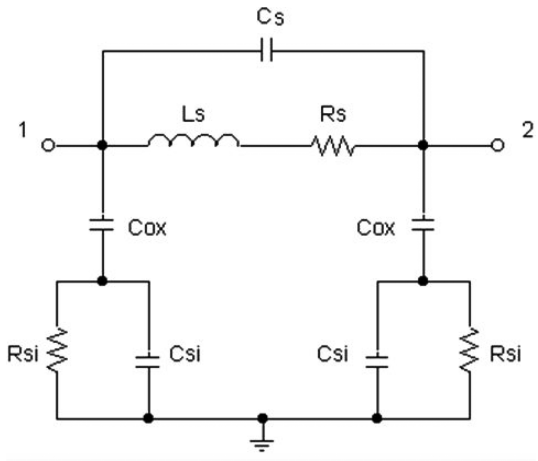

Fig. 2. Equivalent Circuit Model of On-Chip Spiral Inductors.

and the line width and line spacing are 15 μm and 5 μm, respectively. The length of each side of the spiral inductor for L_1, L_2 and L_3 are 67.0 μm, 67.0 μm, and 82.0 μm, respectively.

The equivalent circuit model for an on-chip spiral inductor is shown in Fig. 2 [13]. L_s and R_s are the series inductance and resistance of the spiral, respectively. C_s represents the capacitance between metal traces. C_{ox} is the oxide capacitance from the spiral to the substrate. C_{si} and R_{si} model the substrate capacitance and conductance.

The measured data are plotted in Fig. 3. A maximum $|S_{21}|$ of about −11 dB occurs at 3 GHz and 5 GHz. In a wide bandwidth from 2.5 GHz to 5.5 GHz, $|S_{21}|$ remains above −15 dB.

Here, the vertical coupling of two spiral inductors has been investigated. As shown in Fig. 4, two identical spirals overlap with one on top of the other. The vertical distance between them is about 1 μm. Figure 5 shows the simulation of on-chip spiral inductor. Since the coupling between two vertically coupled spirals is very strong, they

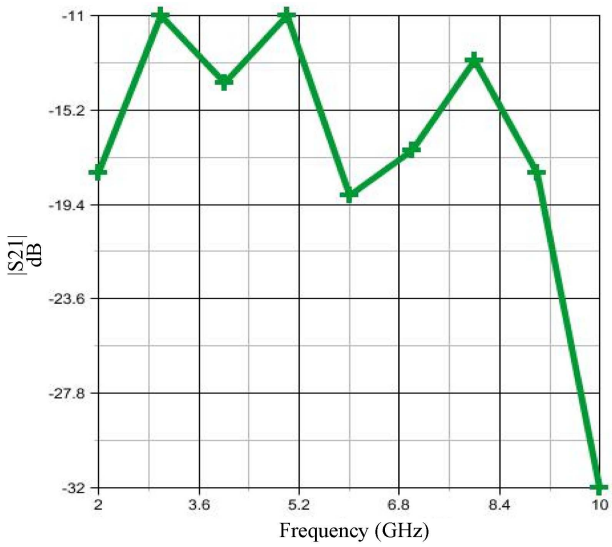

Fig. 3. (Color online) Measured data for Coupled Spirals.

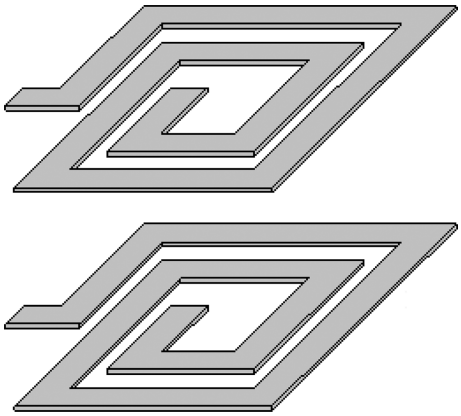

Fig. 4. Vertically Coupled On-Chip Inductors.

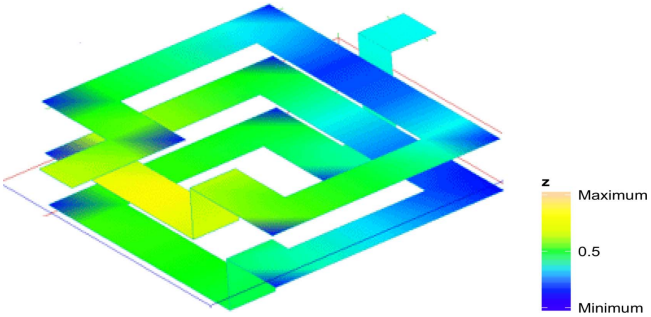

Fig. 5. (Color online) Simulation of On-Chip Inductors.

can be used as an on-chip transformer, especially for heterogeneous integration applications.

4. Coupling between On-Chip Inductors and Transistors

In radio-frequency integrated circuits where passive and active devices coexist on the same chip, spiral inductors can couple a significant amount of electromagnetic energy to sensitive transistors [14]. The on-chip experiment was implemented to investigate the coupling between on-chip inductors and transistors. As shown in Fig. 6, a spiral inductor and a transistor have been laid out side-by-side.

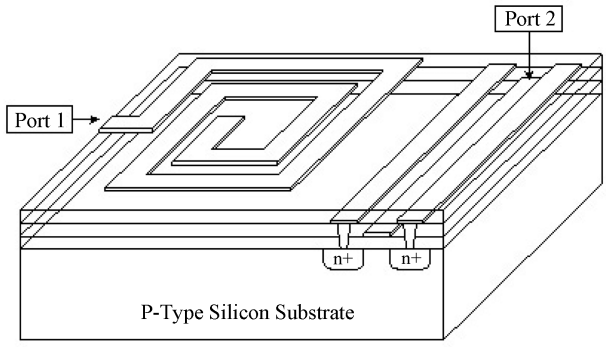

Fig. 6. Coupled Spiral Inductor and Transistor.

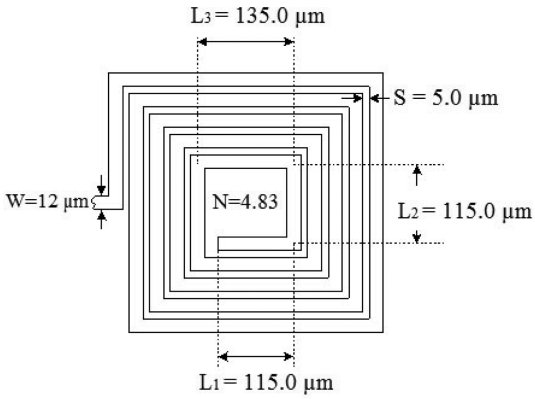

Fig. 7. Physical Dimensions of the Spirals coupled to the Transistor.

The physical dimensions of the spiral are shown in Fig. 7. The total number of turns is 4.83. The line width and line spacing of the conductor are 12 µm and 5.0 µm, respectively. The length of each side of the spiral for L_1, L_2 and L_3 are 115.0 µm, 115.0 µm and 135.0 µm, respectively.

The transistor has a gate width of 250 µm. The experiment compares the coupling effects of two kinds of transistor layout configurations: one has a single gate finger, and the other has multiple gate fingers, as illustrated in Fig. 8 and Fig. 9.

The measured data are plotted in Fig. 10. Both curves show a maximum $|S_{21}|$ of about −19 dB at different frequencies. When the gate width is 250 µm for the single gate finger, the variation of coupling effect is more and the resonance frequency is similar to the multiple gate fingers. But when the gate width is 60 µm for the multiple

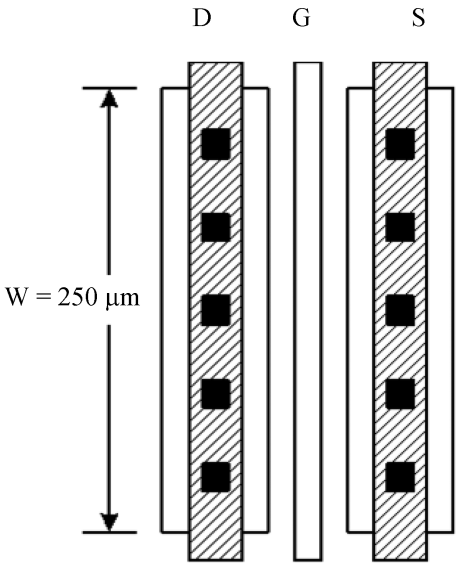

Fig. 8. Layout of Single Gate Finger NMOS Transistors.

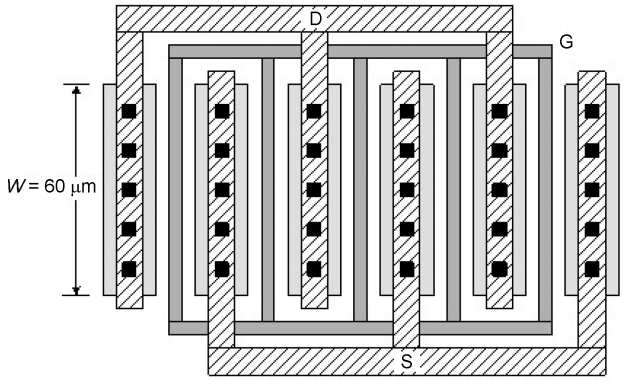

Fig. 9. Layout of Multiple Gate Finger NMOS Transistors.

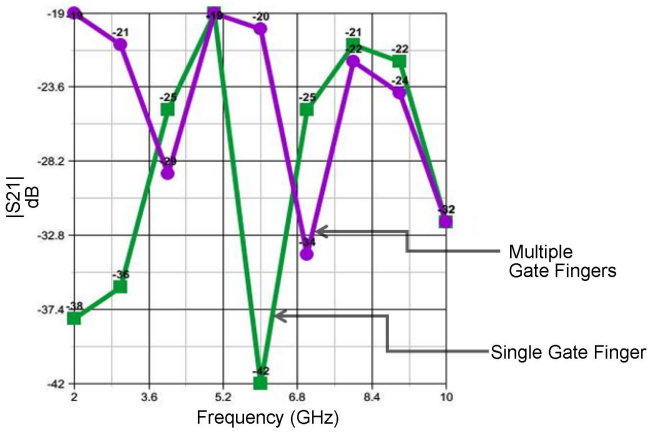

Fig. 10. (Color online) Measured data for NMOS Transistor with Single and Multiple Gate Fingers.

gate finger, the variation in the coupling effect is less and slightly different in the resonance frequency.

5. Results and Discussion

The coupling between spirals and transistors can considerably disturb the performance of analog radio-frequency integrated circuits, particularly that of wireless transceivers. In a monolithic wireless transceiver, on-chip inductors are used in both the low noise amplifier at the input stage and the power amplifier at the output stage. The low noise amplifier typically has a high power gain of about 20 dB; thus, the active transistors in the amplifier should be very extensive, typically up to several hundred microns. The electromagnetic coupling between the inductors and the amplifying transistors can form feedbacks either inside the low noise amplifier or between the low noise amplifier and the power amplifier. Such feedback will degrade the noise performance of the low noise amplifier.

The simulator is based on the Method of Moments technology that is particularly efficient for analyzing spirals and transistors. It is designed to evaluate multi-layer planar geometries and generate the accurate electro-magnetic model. An efficient numerical method is used for calculating semiconductor substrate losses. It is considered by resolving the complex Helmholtz equation via the application of 1D estimation for on-chip inter-connects. The method of modeling on-chip interconnects is extended to characterize integrated inductors by de-composing the spiral into an inductance matrix. A computer model gives exact results compared with the published data, computer-generated by ADS Momentum [17]. Design optimization of spiral inductors is also supported by computer simulation. In this paper, a general methodology for computing the mutual inductance and mutual coupling coefficient of various on-chip spiral inductors and transistors were analyzed, and a good agreement with measurements was found.

6. Conclusion

In this study, an efficient technique for spiral inductor has been developed and tested. A previously developed inductor model was used as the backbone for the optimization calculations, and a procedure was established to carry out the optimization of the layout of the inductors. The approach developed can reduce the design cycle significantly and thus decrease the development cost of radio-frequency integrated circuits. This study investigates some of the radio-frequency effects associated with modern high frequency and high chip density integrated circuits. The modeling provides an alternative way of optimizing on-chip inductors and designing novel inductive

devices. The characterization of on-chip interconnects is used to investigate the high-speed on-chip digital signal transmission. The measured data shows that the on-chip electromagnetic coupling can induce serious problems with the performance of analog radio-frequency integrated circuits.

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